REMARKS

Claims 1-16 are pending. Claims 1-4, 7-10 and 13-15 stand rejected under 35 U.S.C. §103(a) as being unpatentable over United States Patent No. 6,625,756 to Grochowski et al. (Grochowski), filed December 21, 1999, in view of United States Patent No. 6,298,289 to Lloyd et al. (Lloyd), filed April 24, 1999. Claims 5, 6, 11, 12 and 16 are objected to as being dependent upon rejected claims.

In response to the Official Action, amendments are made to the independent claims, claims 1, 7 and 13 in order to make them more specific. The claims as amended avoid the rejection under §35 U.S.C. §103(a).

It is submitted that Claims 1-4, 7-10 and 13-15 as amended are allowable by virtue of their unique recitations. It is submitted that allowability of the previously rejected claims obviates the Examiner's objection as to claims 5, 6, 11, 12 and 16.

Overview of the Invention

Applicant will first qualitatively describe features of the present invention which provide for significant operational advantages, and then relate these features to specific recitations in the claims. As pointed out by Applicant in paragraphs [0002] through [0005], microprocessors, for example, are utilized in environments in which it is a virtual certainty that ionizing radiation will cause processor errors. A radiation hardened processor can be used to avoid such errors. However, radiation hardened

processors tend to lag non-hardened processors by two to three generations in such areas as speed and capacity.

Applicant provides, as explained at paragraph [0012] for example, an arrangement in which a non-hardened processor is utilized in a fault tolerant system. A redundancy technique is utilized including steps in which the non-hardened processor calculates a result based on an original instruction and a result based on a mirror instruction. A result produced in response to the original instruction during a first time is compared to a result produced in response to the mirror instruction during a separate time period. Applicant uses a radiation hardened comparator. If the comparison indicates a difference, occurrence of an error is detected. The system responds to detection of an error so that the occurrence of the error can be tolerated. Applicant thus provides for reliable operation in an environment subject to errors induced by ionizing radiation while being able to use a processor that is not radiation hardened.

The Claims

Independent claims 1 and 7, and, consequently, the claims respectively dependent thereon, have been amended to specifically point out that the processor is not hardened. This recitation is supported, for example in the first line of paragraph [0012] which refers to, "a non-hardened processor." Claims 13 and, consequently, the claims dependent thereon have been amended to specifically

point out that calculations that produce values to be compared are produced in the processor. The values are sent to the hardened comparator. Comparison is performed in the hardened comparator. Values indicative of the results of comparisons are sent back to the processor. All claims have been amended to point out the compared results from the original and mirror instructions are produced during separate time periods. This recitation is supported, for example, in paragraph [0011] where time redundancy operation is specified. This recitation is further supported by the description of circuitry details in paragraph [0026], which explains that one comparator input is coupled through a delay line.

The Rejection Under 35 U.S.C. §103(a)

Claims 1-4, 7-10 and 13-15 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Grochowski in view of Lloyd. In short, the rejection states that Grochowski includes a processor to execute an original and mirror instructions and comparison circuit to compare an original result with a first mirror result. Agreement or disagreement of the compared values defines a first or a second state. Lloyd discloses a radiation hardened processor "prepared for SEU errors." The rejection states that. "It would have been obvious to one skilled in the art at the time of the invention to use the additional reliability aspects of Lloyd in the invention of Grochowski." Further features are cited against the dependent apparatus claims. Method claims 7-10 and claims 13-15 to a programmed medium are effectively rejected on similar ground.

Accepting these premises for the sake of the present discussion, neither Grochowski nor Lloyd teaches or suggests what Applicant has claimed. Grochowski is not effective as a base reference. Lloyd does indeed provide teachings that can be combined with Grochowski. However, what Lloyd teaches does not provide the recitations in Applicant's claims that are missing from Grochowski's teachings. The rejected claims as filed, and even more explicitly as amended, recite structure and operation that is not present in the cited references.

Teachings of the References

-Original and Mirror Circuit Instruction Processing

Grochowski is entitled, "Replay Mechanism For Soft Error Recovery." Gruchowski utilizes a different form of redundancy than that recited by Applicant. At column 4, lines 40-53, Grochowski states, "FIG. 2A is a block diagram of one embodiment of processor 110 (processor 210) that supports soft error detection through redundant execution clusters. Processor 210 includes a pair of execution cores 216(a), 216(b) (generically, execution core 216), which are operated in lock step. Each execution core 216 includes a replay unit 170 (170(a) and 170(b)) and an execution unit 280 (280(a) and 280(b)). Identical instructions are provided to replay unit 170 by, e.g. a fetch unit (not shown). ... Results generated by execution units 280 are compared by check unit 160 and a discrepancy indicates a soft error may have occurred."

In the claims as filed, Applicant recites that each of the redundant results are produced by one processor. Grochowski utilizes first and second execution cores. To even more explicitly point out his structure, method and program, Applicant has specified in the claims as amended that the processor compares an original and a mirror calculation result which are each produced in a separate time period. This is recited at Claim 1, lines 4-5, Claim 7, lines 4-5, and Claim 13, lines 6-7. This structure and operation enables the uses of a single processor rather than the two processors disclosed in Figure 2, for example, of Grochowski. It is therefore submitted that Grochowski does not serve as a base reference with respect to a time redundant system and method as recited by Applicant.

Lloyd does not disclose use of a single processor. At column 10, lines 42-51, Lloyd states, "The present invention employs Single Event Upset (SEU) mitigation features in the preferred embodiment. Table 1 identifies the SEU mitigation approaches that may be used in present invention. The large amount of storage in the CPU subunit 12 makes this subunit the largest contributor to SEU effects in the integrated SCE 10. To protect against SEUs in the PowerPC.TM. 750 microprocessor 18, the three microprocessors 18a, 18b, 18c are voted together, as mentioned above. The three microprocessors 18a-8c are operated in parallel, and outputs are compared cycle-by-cycle cycle." Lloyd's technique is known as triple modular redundancy (TMR). TMR is discussed in Applicant's specification at paragraph [0006]. The technique taught by Lloyd is one that Applicant explicitly wishes to avoid. The above cited recitations in

claims 1, 7 and 13 provide for comparison of results produced during different time periods. Lloyd explicitly states in the passage quoted above that the results are compared cycle by cycle. This is expressly contrary to Applicant's recitations. Lloyd must perform three computations 100% percent of the time. Applicant points out at the end of paragraph [0023] of his specification that is not necessary to perform the third calculation 99% of the time. This advantage directly and necessarily results from Applicant's recited structure and operation.

-Radiation Hardened Processor

The rejection states that Lloyd discloses a radiation hardened processor. This is correct. However, this is not what Applicant claims. Applicant in the claims as filed points out that a comparison is performed in a radiation hardened comparator. The claims as amended even more explicitly point out that distinguishing structure. Claim 1, lines 1-2 and Claim 7, lines 2-3 state that processor, the component which performs the calculations, is not radiation hardened. Claim 13, lines 6-7 more explicitly recite that the comparison is done in the radiation hardened component and that calculations are not performed in the radiation hardened component.

At column 7, lines 14-15, Lloyd states, "The microprocessor 18 is radiation hardened to >60K rads and is latchup immune." This is expressly contrary to what Applicant recites. In paragraph [0005] of his specification, Applicant explains that using a radiation hardened microprocessor provides significant disadvantages.

Requirements of the MPEP for a Rejection Under 35 U.S.C. §103(a)

MPEP 2143.03 states that all limitations of a claim must be met in order to make out a rejection under 35 U.S.C. §103(a). Neither Grochowski nor Lloyd discloses comparing results produced in separate time periods based on an original and a mirror instruction. Neither Grochowski nor Lloyd disclose a non-hardened processor in conjunction with a hardened comparator. It is therefore submitted that the rejection under 35 U.S.C. §103(a) merits withdrawal on this basis.

Under MPEP 2143.01, "In determining the propriety of the Patent Office case for obviousness in the first instance, it is necessary to ascertain whether or not the reference teachings would appear to be sufficient for one of ordinary skill in the relevant art having the reference before him to make the proposed substitution, combination, or other modification." In the present case, Applicant points out that his processor is the component that performs calculations, and explicitly recites that his processor is not radiation hardened. Lloyd explicitly teaches that his processor is radiation hardened. It is submitted that one skilled in the art would not be led by the teachings of a reference to provide a structure with is contrary to that taught by the reference. It is therefore submitted that the rejection under 35 U.S.C. §103(a)does not meet the requirements of MPEP 2143.01.

Under MPEP 2142, for a rejection under 35 U.S.C. §103(a), there must be a suggestion in the art to provide the claimed invention. Applicant's own disclosure

cannot be used as a source of teachings. Again, Lloyd's teaching of a radiation hardened processor is not a suggestion in the art of the use of a non-radiation hardened processor. Also, Lloyd teaches triple modular redundancy. Applicant expressly states that he wishes not to employ this technique. It is submitted that one skilled in the art would thus not be led by Lloyd's teaching to do what Applicant has done.

It is therefore submitted that the rejection under 35 U.S.C. §103(a) merits withdrawal.

Summary

It is submitted that Claims 1-4, 7-10 and 13-15 as amended explicitly recite subject matter neither taught not suggested by the art of record. It is submitted that allowability of the previously rejected claims obviates the Examiner's objection as to claims 5, 6, 11, 12 and 16.

Applicant has demonstrated that the references do not include each limitation found in the claims. It is therefore submitted that the rejection under 35 U.S.C. §103(a) should be withdrawn on this basis. Applicant has also demonstrated that Grochowski is not suitable as base reference with respect to a time redundant system and that Lloyd does not disclose a non-hardened processor which performs calculations providing results to a radiation hardened comparator. It is submitted that the rejection under 35 U.S.C. §103(a) merits withdrawal on this ground as well.

In view of the foregoing, Applicant respectfully submits that the application is now in condition for allowance. If it is believed that the application is not in condition for allowance, the Examiner is respectfully requested to contact the undersigned to expedite the prosecution of the application.

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